1.6Gb/s 16-LEVEL SUPERPOSED APSK MODEM WITH BASEBAND SIGNAL PROCESSING COHERENT DEMODULATOR

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ABSTRACT

A 1.6Gb/s 16-level superposed APSK MODEM using newly developed baseband signal processing coherent demodulator is described. The MODEM has much improved performance characteristics while having much simplified configuration comparing with the already reported one.

Jitter power of the recovered carrier is less than -36dB and required C1/N for BER of 10^{-9} is better than 25.4dB through the MODEM loop back test (BT = 1.35).

Introduction

MAPSK (Multiple Amplitude and Phase Shift Keying) is considered to be an advantageous means for effective use of the transmission frequency band and the feasibility of realizing APSK MODEM for use in microwave digital transmission systems has been studied recently. Of several APSK methods, the method in which 16-level signals are arranged in a lattice form on the signal space has attracted a particular attention because of its high transmission efficiency and some concrete studies have been conducted.

Superposed modulator and demodulator APSK has been proposed as a means for realizing high performance 16-level APSK transmission[1] and one of the authors has reported an experimental study of a 1.6Gb/s APSK MODEM and its feasibility[2].

Although MAPSK has a merit of effective use of signal space, it provides a demerit of being subject to degradation because of various distortions and incompleteness of demodulator in use. Accordingly, it is the major object in realizing hardware to minimize distortion caused in the signal processing in the demodulator. It is also aimed to realize such a carrier regeneration circuit as capable of reproducing the carrier containing less steady-state phase error and pattern jitter. The higher the modulation speed, the more difficult it is to realize such hardware having these characteristics.

A newly devised demodulator features a simple construction, high-speed performance and high immunity against transmission distortion. Its excellent performance has been verified both theoretically and experimentally.

The configuration of the new modulation-demodulation system and the performance of the engineering model for 400MB 16-level (1.6Gb/s) APSK signal are described.

Modulation

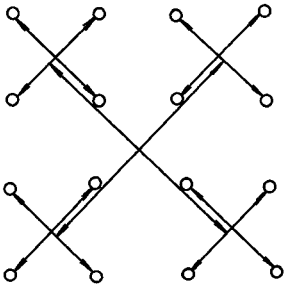
In the modulator 16 signal points are arranged in lattice form on a signal space by superimposing a 4-phase PSK signal (2nd path signal) on another 4-phase PSK signal (1st path signal). Here, the signal level of the 2nd path is made a half that of the 1st path. The process of modulation and the configuration of the modulator are shown in Fig. 1. With this configuration incorporating identical circuits connected in parallel, high-accuracy and high-stability signals are obtainable at high data rate as well.

Demodulation

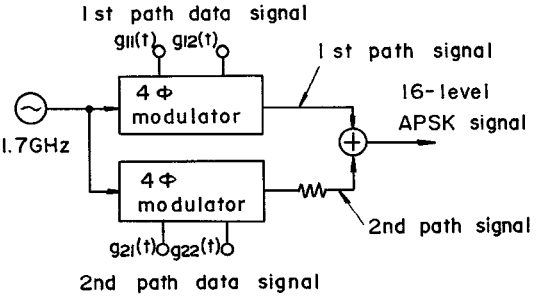
In 16-level superposed APSK, signal points are arranged more closely on the signal space than in 4-phase PSK, so that it is necessary to extremely diminish the phase error of the recovered reference carrier for coherent detection.

The phase error of the recovered reference carrier includes 1) steady-state phase error ascribable to the frequency variation of the transmitting and receiving local oscillators, 2) orthogonality deviation of the modulator and demodulator and 3) pattern jitter inherent to circuit configuration and caused by circuit incompleteness of the carrier recovery circuit. It is comparatively easy to reduce the first type of phase error by selection of proper loop parameters or addition of an external control circuit. However, the third type of phase error shall be eliminated by developing such circuitry that will not, on principle, cause pattern jitter.

The demodulator shown in Fig. 2 has been newly devised in consideration of the abovementioned requirements. Data signal regeneration is performed by a feed-forward quantizer which consists of two stages of units. Each unit quantizer consists of a data regenerator, a low pass filter and a subtractor. The VCO control signal $\varepsilon(t)$ is obtained by processing two first path regenerated data and two quantizing error signals of second stage quantizer units, as shown in Fig.2.



(a) Signal constellation.



(b) Block diagram.

Figure 1. Superposed APSK modulator.

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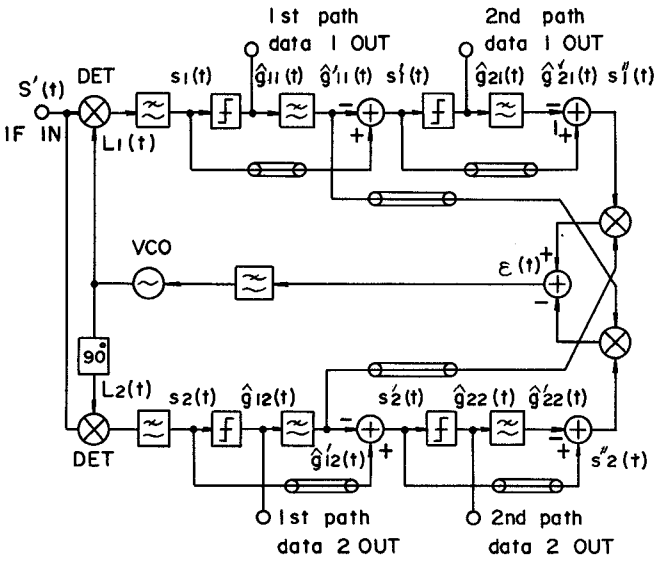

Figure 2. Block diagram of demodulator.

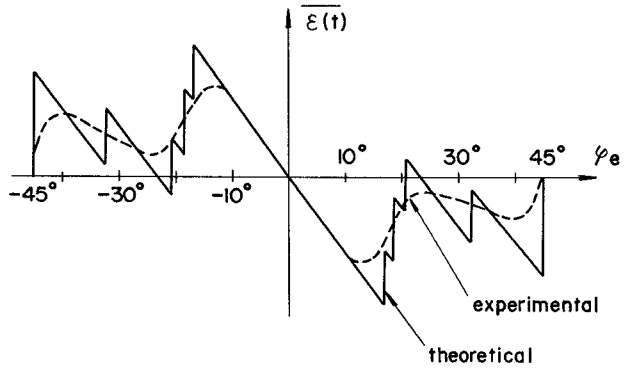

Figure 3. Equivalent phase detector characteristic of carrier recovery loop.

Since ε(t) with an extremely small noise is obtainable at the neighborhood of the stable point as stated later, the pattern jitter of the VCO output signal or the recovered carrier can be made extremely small. The use of a low-pass filter equivalent to the transmission path for waveform shaping of the quantized signal allows the transient noise of the quantizing error signal to be extremely small.

When the transmission path has a even-symmetrical frequency characteristic around the center frequency, the control signal of the VCO, ε(t),is given by

$$\varepsilon(t) \triangleq S''_1(t)\cdot g'_{12}(t) - S''_2(t)\cdot g'_{11}(t)$$
$$= -\{g'^2_{11}(t) + g'^2_{12}(t) + \frac{1}{2}g'_{11}(t)\cdot g'_{22}(t) + \frac{1}{2}g'_{12}(t)\cdot g'_{21}(t)\}\sin\phi e - \frac{1}{2}\{g'_{12}(t)\cdot g'_{21}(t) - g'_{11}(t)\cdot g'_{22}(t)\}(\cos\phi e - 1) \quad \ldots (1),$$

where g'ij(t) is the response given when data signal gij(t) is passed through the low-pass filter having a frequency characteristic equivalent to that of the transmission path and φe is the phase error of the reference carrier. The effect of thermal noise which may be added to the signal in the transmission path is neglected in the equation for simplicity.

From Equation(1), when $g_{ij}(t)$ is a random signal having mean value of zero, ε(t)= -2 sinφe, and the second term shows a noise component of the VCO control signal. When phase error φe is small (φe<<1), the noise level is extremely small. As a result, the jitter power of the reference carrier can be made extremely small without providing any particular jitter suppression circuit.

The equivalent phase detector characteristic of the carrier recovery loop is shown in Fig.3. The undesired stable points near 23° on the theoretical curve shown in the figure can not be stable in actual system. This is because,near these points, ε(t) contains a great amount of noise due to the modulating data signal. This is verified by experimental data shown by the dotted line in Fig. 3.

As stated above, this method substantially provides a much reduced pattern jitter in the recovered reference carrier. Moreover, its process of obtaining the phase error voltage includes the process of regenerating the data signal, so that its circuit configuration is very simple. In addition, because one input signal to the multiplier is a quantizing error signal, the required operating range of the multiplier is small, which is very advantageous for realizing intended circuitry.

Performance of Experimental MODEM

A 16-level APSK MODEM using a carrier frequency of 1.7GHz and a transmission capacity of 1.6Gb/s has been implemented for experimental purpose. Table 1 gives the major design parameters and characteristics of the MODEM.

Modulator

Each 4-phase modulator in Fig.1 consists of two 1.7GHz ring modulators. The major characteristics of each 4-phase modulator are as follows. Modulation phase error: within ±1.5°. Modulation amplitude deviation: within ±0.2dB. Rise time: less than 0.7nS. Pulse width variation: less than ±75pS. Fig.4 shows the signal constellation of the superposed APSK signal

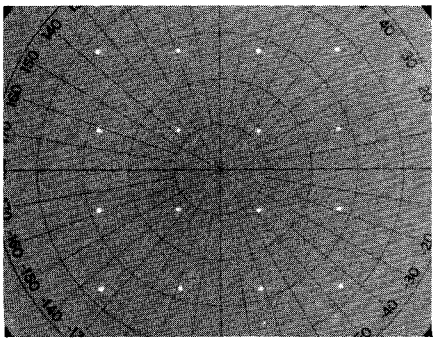

Figure 4. Signal constellation of superposed APSK signals.

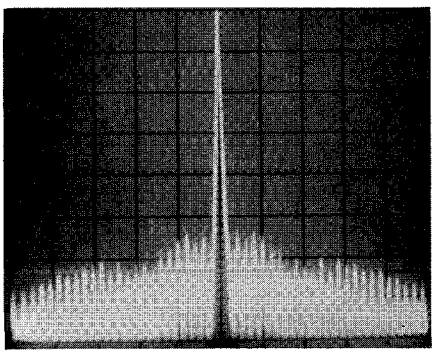

Figure 5. Power spectrum of recovered reference carrier.

Table 1. Design parameters and characteristics.

Carrier frequency	1700 MHz
Clock frequency	400 MHz
Data rate	1.6Gb/s
Required C1/N for BER $1x10^{-9}$	25.4 dB
Carrier jitter	-36 dB
Loop gain	$4.0x10^{8}$ Hz
Noise band	$1.5x10^{6}$ Hz
Damping factor	0.7

measured by a network analyzer, and an extremely high accuracy signal arrangement is achieved. The pulse width variation of the modulated carrier is less than ±100 pS.

Demodulator

The double balanced mixer is used as the coherent detector for demodulation. The detector has a wideband characteristic over 1.7GHz ±400MHz, and a sufficient linearity for amplitude variation as well as for phase variation. A high-sensitivity and high-speed data regenerator is constructed by using a wideband DC amplifier and an ultrahigh-speed flipflop. The ambiguous discrimination width of the data regenerator is 6% of the eye opening of the demodulated signal. The analog multiplier using a balanced difference circuit with twin transistors of f_T=6GHz provides sufficient accuracy and stability, which is formed on an alumina-ceramic substrate as a hybrid IC.

The carrier recovery circuit uses the main loop mentioned in the preceding paragraph and a subloop of an astatic control circuit, so that steady-state phase error due to center frequency variation of the input modulating signal and free running frequency variation of the VCO can be suppressed. The loop parameters are shown in Table 1.

Characteristics of Demodulation System

The modulating data signals for MODEM loopback

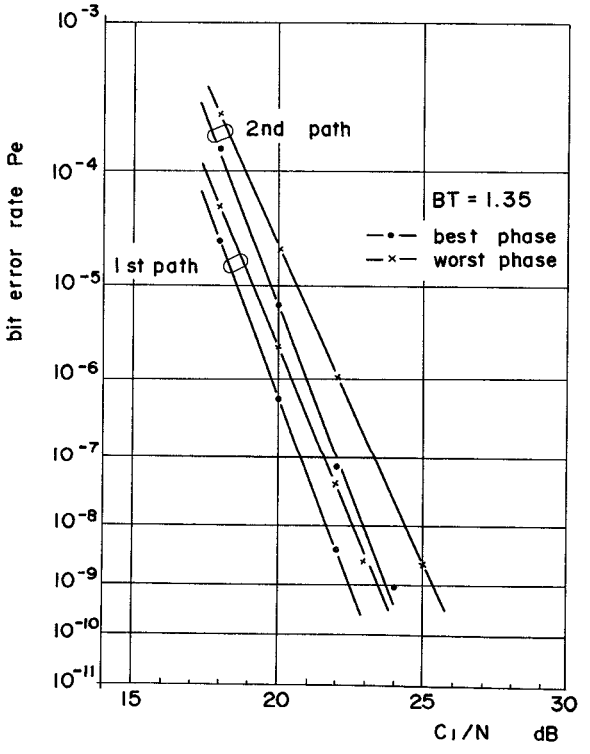

Figure 6. Bit error rate characteristics.

test are the 11 stage and 15 stage maximum length PN sequences. To simulate the transmission path, a 5-stage Thomson band-pass filter (BT = 1.35) is employed.

Fig.5 shows the power spectrum of the recovered carrier. It is to be noted that the noise power is extremely small. The noise power observed was less than -36dB below the recovered carrier power. This provides an excellent result as examined theoretically in the preceding paragraph. In this phase lock loop no false lock phenomenon as expected was observed. This loop is verified to perform a stable pull-in operation in the range of C1/N≥18dB (C1 is the unmodulated carrier power of the 1st path signal.)

The bit error rate characteristic obtained by the loopback test of the MODEM is shown in Fig.6. The worst value of C1/N for the bit error rate of 1×10^{-9} was 25.4dB. These performance characteristics of the MODEM show that the MODEM is much improved when compared with the reported one,[2] while it is simpler in circuit configuration. Further improvement in bit error rate characteristic will be achievable by improving impedance matching between circuits.

Performance characteristic degradation due to the incompleteness of the transmission path or MODEM circuit has been studied and measured for some incomplete properties by using this MODEM. The data tells that to keep bit error rate degradation to be less than twice as much as the value shown in Fig.6 requires that the input signal level variation of the demodulator, the phase error of the clock signal for data signal regeneration, and the threshold level variation of the data regenerator, should be within ±0.2dB, within ±10 degrees, and within 2% of the peak to peak value of the demodulated signal respectively.

Loop Back Test through Millimeter Wave Transmitter-Receiver

Loop back test has been conducted through 50GHz transmitter-receiver. The test result shows that the degradation of required C1/N value giving the bit error rate of 10^{-9} is less than 1.5dB, compared to the MODEM loop back test.

Conclusion

A 1.6Gb/s 16-level superposed APSK MODEM based on a new operating principle has been developed and manufactured on a trial basis. The MODEM is shown to be very simple in circuit configuration, and easy to construct. The excellent performance in such a high-speed region as 1.6Gb/S is shown both theoretically and experimentally.

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